COMMENTS

I. Status of claims

Claims 3-23 were pending. Claims 4-6, 10, and 25 have been amended. Claims 31-33 have been added.

II. Claim Rejections under 35 U.S.C. § 102(e)

The Examiner has rejected claims 13 and 25 under 35 U.S.C. § 102(e) over Jewell (US 6,243,508). In particular, the Examiner has indicated that (emphasis added):

> Jewell et al. discloses an optoelectronic device comprising an optical lens system comprising a lens substrate 12 supporting one or more optical lenses 24 and a semiconductor (silicon) spacer substrate 132 defining one or more apertures 133 therethrough; an optical device system comprising a device substrate supporting one or more optical devices 26'; wherein the lens substrate 12 is bonded to the silicon spacer substrate 132 and the silicon spacer substrate 132 is bonded to the device substrate supporting one or more optical devices 26', with the one or more optical lenses 24, the one or more optical devices 26' held together in registered alignment. Note figure 17 of Jewell et al.

Contrary to the Examiner's assertion, however, the circuit layer 132 shown in FIG. 17 of Jewell does not constitute a spacer substrate. Jewell's only teaching regarding the nature of "circuit layer 132 is as follows:

> In a preferred embodiment, circuit layer 132 comprises deposited silicon in a polycrystalline or crystalline state. ... (Col. 14, lines 58-60).

> In a preferred embodiment, wafer 12 is sapphire, circuit layer 132 is silicon-on-sapphire (SOS), and the functions of monitoring the output of transmitting optoelectronic transducer 26, driving transducer 26, and amplifying the output of receiving optoelectronic transducer 26', are all integrated into circuitry formed in circuit layer 132. (Col. 15, lines 14-20)

In interpreting claims, the general rule is that terms in the claims are to be given their ordinary and accustomed meaning. A "substrate" is a well-known term of art of that refers to

the foundation or supporting base material on which a device or other structure is fabricated or assembled. A deposited "layer" on the other hand refers to a thin film of material that is deposited on a substrate. Silicon-on-sapphire is a well-known technology that involves forming circuits from n- and p- channel transistors that consist of thin epitaxial islands of silicon grown on a sapphire substrate. Accordingly, based on Jewell's teaching that circuit layer 132 comprises polycrystalline or crystalline silicon deposited on wafer 12 (e.g., silicon-on-sapphire), one of ordinary skill in the art at the time of the invention, having knowledge of the ordinary and accustomed meaning of the term "substrate", would not reasonably have concluded that Jewell's circuit layer 132 was a "substrate".

In addition, the term "bonded", when used in the context of one substrate bonded to another substrate, has an ordinary and accustomed meaning in the art that refers to a bonding state in which an intermediate bonding region exists between the two substrates that is distinguishable from the ordered chemical bonds formed between a layer of polycrystalline or crystalline silicon deposited on a substrate. Accordingly, one of ordinary skill in the art at the time of the invention, having knowledge of the ordinary and accustomed meaning of the term "bonded", would not reasonably have concluded that Jewell's circuit layer 132 was "bonded" to wafer 12.

Therefore, since Jewell's connector does not contain a spacer substrate, much less a spacer substrate bonded to a lens substrate, the Examiner's rejection of claim 13 under 35 U.S.C. § 102(e) over Jewell should be withdrawn.

Claim 25 incorporates the features of independent claim 13 and therefore is patentable for at least the same reasons. Claim 25 also is patentable for the following additional reason.

Claim 25 now requires that each of the spacer substrate apertures has a lens substrate opening at a surface facing the lens substrate and a device substrate opening at a surface facing the device substrate, wherein for each spacer substrate aperture the lens substrate opening is larger than the device substrate opening. Jewell does not teach or suggest such a feature. Indeed, in FIG. 17 Jewell clearly shows that the openings at both ends of void 133 are the same size.

III. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 3-12, 21-24, and 26-30 under 35 U.S.C. § 103(a) over Jewell.

A. Claims 3 and 28

Independent claim 3 recites that the optical lens system comprises a device bonding surface supporting a solderable metallization pattern and one or more optical lenses that are recessed below the device bonding surface, and that a plurality of solder bumps bond an optical device substrate to the device bonding surface.

The Examiner has asserted that Jewell discloses in FIG. 17 an optoelectronic device in which "one or more optical lenses 24 are recessed below the device bonding surface of the silicon spacer substrate 132." Contrary to the Examiner's assertion, however, there are no optical lenses recessed below the surface of Jewell's circuit layer 132. Instead, the optical lenses 24 protrude from a lens layer 130 that is located on a surface of wafer 12 that is opposite the surface on which circuit layer 132 is deposited. When read in the light of applicants' specification, there is no reasonable interpretation of the word "recessed" that would have led one of ordinary skill in the art at the time of the invention to conclude that lenses 24 are recessed below a device bonding surface of circuit layer 132.

For at least this reason, the Examiner's rejection of independent claim 3 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claim 28 incorporates the features of independent claim 3 and therefore is patentable for at least the same reasons.

B. Claims 4-10, 12, and 21-24

Independent claim 4 has been amended and now requires "an optical lens system comprising one or more optical lenses incorporated into an optical substrate bonded to a spacer substrate." As explained above in connection with claim 3, Jewell's connector does not contain a spacer substrate, much less a spacer substrate bonded to a lens substrate.

Therefore, for at least these reasons, the Examiner's rejection of claim 4 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claims 5-10, 12, and 21-24 incorporate the features of independent claim 4 and, therefore, these claims are patentable for at least the same reasons. Claims 5-7, 21, and 22 are patentable for the following additional reasons.

Claim 5 requires a wafer bond that bonds the optical substrate to the spacer substrate and claim 6 requires a solder bond that bonds the optical substrate to the spacer substrate. The Examiner has indicated that:

> With regard to claims 5, 6, 10, Jewell et al. does not disclose the optical substrate is bonded to the spacer substrate 132 by a wafer bonding process or a flip-chip solder bonding process. However, Applicants' claims 5, 6, 10 do not distinguish over the Jewell et al. reference regardless of the process used to bond the substrates together, because only the final produce if relevant, not the process of making such as wafer bonding process or flip-chip bonding process.

Claims 5 and 6, however, now call for specific bonds (namely, a wafer bond and a solder bond) that are readily distinguishable from the epitaxial bonds between Jewell's polycrystalline (or crystalline) silicon circuit layer 132 and wafer 12. Moreover, based on Jewell's teaching that circuit layer 132 corresponds to a deposited polycrystalline or crystalline layer of silicon, one of ordinary skill in the art at the time of the invention would not reasonably have been motivated to bond circuit layer 132 to wafer 12 with a wafer bond or a solder bond. For at least these additional reasons, the Examiner's rejection of claims 5 and 6 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claim 7 recites that "the thickness of the spacer substrate is selected based upon a representative focal distance between the one or more optical devices and the one or more optical lenses." The Examiner has failed to address the features of claim 7. Moreover, Jewell does not teach or suggest anything about the thickness of circuit layer 132. For at least these additional reasons, the Examiner's rejection of claim 7 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claim 21 recites that "the one or more optical lenses are incorporated into the device bonding surface." The Examiner has indicated that Jewell discloses in FIG. 17 an optoelectronic device in which "the one or more optical lenses 24 are recessed below the device bonding surface of the silicon spacer substrate 132 and incorporated in the optical lens

system 12." As explained above, however, the optical lenses 24 protrude from a lens layer 130 that is located on a surface of wafer 12 that is opposite the surface on which circuit layer 132 is deposited. When read in the light of applicants' specification, there is no reasonable interpretation of the claim language "incorporated into" that would have led one of ordinary skill in the art at the time of the invention to have concluded that lenses 24 are incorporated into a device bonding surface of circuit layer 132. For at least these additional reasons, the Examiner's rejection of claim 21 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

Claim 22 recites that "the one or more optical lenses are recessed below the device bonding surface." As explained above, contrary to the Examiner's assertion, there are no optical lenses recessed below the surface of Jewell's circuit layer 132. Instead, the optical lenses 24 protrude from a lens layer 130 that is located on a surface of wafer 12 that is opposite the surface on which circuit layer 132 is formed. When read in the light of applicants' specification, there is no reasonable interpretation of the word "recessed" that would have led one of ordinary skill in the art at the time of the invention to conclude that lenses 24 are recessed below a device bonding surface of circuit layer 132. For at least these additional reasons, the Examiner's rejection of claim 22 under 35 U.S.C. § 103(a) over Jewell should be withdrawn.

C. Claims 11 and 29

Independent claim 11 requires "a plurality of solder bumps disposed between the metallization patterns of the optical device system and the optical lens system, wherein the plurality of solder bumps bond the optical device substrate to the device bonding surface with the one or more optical devices aligned with the one or more optical lenses, and, wherein a characteristic dimension of the plurality of solder bumps is selected based upon a representative focal distance between the one or more optical devices and the one or more optical lenses." The Examiner has asserted that "a characteristic dimension of the plurality of solder bumps 148 is selected based upon a representative focal distance between the one or more optical devices 26' and the one or more optical lenses 24." However, contrary to the Examiner's assertion, Jewell fails to teach or suggest anything about the dimensions of bump bonds 148. For at least these reasons, the Examiner's rejection of claim 11 under 35 U.S.C. § 103(a) should be withdrawn.

Claim 29 incorporates the features of independent claim 11 and therefore is patentable for at least the same reasons.

D. Claims 26, 27, and 30

Claims 26, 27, and 30 incorporate the features of independent claim 13 and, therefore, these claims are patentable for at least the same reasons explained above.

IV. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-1078.

Respectfully submitted,

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Edouard Garcia
Reg. No. 38,461
Telephone No.: (650) 631-6591

Please direct all correspondence to:

Agilent Technologies, Inc.
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

APPENDIX

Marked-up versions of the amendments made by the Response to the Office action dated May 8, 2003, are presented below.

In the claims:

4. (Twice Amended) An optoelectronic device, comprising:

an optical device system comprising an optical device substrate supporting one or more optical devices and a solderable metallization pattern having a spatial arrangement with respect to the one or more optical devices;

an optical lens system comprising one or more optical lenses incorporated into an optical substrate bonded to a spacer substrate having [and] a device bonding surface supporting a solderable metallization pattern having a spatial arrangement with respect to the one or more optical lenses [, wherein the optical lens system comprises an optical substrate incorporating the one or more lenses and the device bonding surface defines one face of a spacer substrate]; and

a plurality of solder bumps disposed between the metallization patterns of the optical device system and the optical lens system;

wherein the plurality of solder bumps bond the optical device substrate to the device bonding surface with the one or more optical devices aligned with the one or more optical lenses.

5. (Amended) The optoelectronic device of claim 4, wherein a wafer bond bonds the optical substrate [is bonded] to the spacer substrate [by a wafer bonding process].

6. (Amended) The optoelectronic device of claim 4, wherein a solder bond bonds the optical substrate [is bonded] to the spacer substrate [by a flip-chip solder bonding process].

10. (Amended) The optoelectronic device of claim 4, further comprising an integrated circuit bonded to the spacer substrate by a flip-chip solder bond [bonding process] and configured to drive the one or more optical devices.

25. (Amended) The optoelectronic device of claim 13, wherein each of the spacer substrate apertures has a lens substrate opening at a surface facing the lens substrate and a device substrate opening at a surface facing the device substrate, wherein for each spacer substrate aperture the lens substrate opening is larger than the device substrate opening [the one or more optical lenses are recessed below the device bonding surface].